



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Image
2811

Applicant: Shanjen Pan et al.

Art Unit: 2811

Serial No.: 09/998,606

Examiner: C. Q. Nguyen

Filing Date: 11/30/2001

Docket No.: TI-31192

Customer No.: 23494

Conf. No.: 4902

Title: HIGH DENSITY CAPACITOR USING TOPOGRAPHIC SURFACE

Petition to Withdraw Holding of Abandonment under 37 C.F.R. §1.181(a)

April 8, 2004

MAILING CERTIFICATE UNDER 37 C.F.R. 1.8(a)

I hereby certify, that on this date, this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

4-8-04

Date

Marianna Smith

Marianna Smith

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

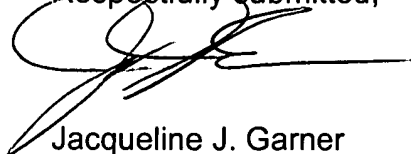
Applicant hereby petitions for withdrawal of the holding of abandonment in the above-referenced patent application. The above-reference patent application was abandoned on 02/27/2004 by the Examiner due to Applicant's failure to file a proper reply to the Office Action dated 07/28/2003 – no reply was received. However, a proper response was sent by facsimile to Technology Center 2800, facsimile number 703-872-9306 on January 27, 2004 and an Auto-Reply Facsimile Transmission was received. Copies of the Facsimile Cover Sheet, Amendment After Final, Request for Extension of Time, the Transmission Verification Report, as well as the Auto-Reply Facsimile Transmission are

attached. Accordingly, the holding of abandonment is improper and should be withdrawn.

If necessary, the Commissioner is hereby authorized to charge any necessary fees to Deposit Account no. 20-0668.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(214) 532-9348
Fax: (972) 917-4418

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'J. Garner', written over a horizontal line.

Jacqueline J. Garner
Reg. No. 36,144

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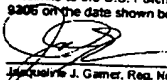
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Jan 27 04 10:08a	Jacqueline J Garner	972-278-9775	P.1
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From:	Jacqueline J. Garner Texse Instruments Incorporated Facsimile: 972-917-4418 Phone: 214-532-9348	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	09/998,606	Confirmation No.	4902
Applicant:	Shanjen Pan et al	TC/A.U.:	2811
Filed:	11/30/2001	Examiner:	C. Q. Nguyen
Docket No.:	T1-31182	Customer No.:	23494
Title:	HIGH DENSITY CAPACITOR USING TOPOGRAPHIC SURFACE		

CERTIFICATION OF FACSIMILE TRANSMISSION	
I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on the date shown below:	
 Jacqueline J. Garner, Reg. No. 38,144	January 27, 2004 Date

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NAME OF INVENTOR(S) Pan et al TITLE OF INVENTION HIGH DENSITY CAPACITOR App. Docket T1-31182 DEPOSIT ACCT NO: 20-0688 FAXED: 1/27/2004 DUE: 10/28/2003 ATTY/SECY: JG	RECEIPT SENT BY TELEPHONE NO: Serial No.: 09/998,606 Filing Date: 11/30/2001 Conf. No.: 4902

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Texse Instruments Incorporated
PO Box 66474, M/S 3638
Dallas, TX 75274

PAGE 17 * RCVDT 01/27/2004 11:06:44 AM Eastern Standard Time * TXN: 0170-0730 * IN * DUE: 01/28/2004 * CNO: 0170-0730 * DUE: 01/28/2004 (mm-ss) 02-39

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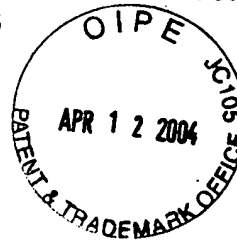
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Facsimile: 972-917-4418
Phone: 214-532-9348



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.: 09/998,606 Confirmation No. 4902
Applicant: Shanjen Pan et al. TC/A.U.: 2811
Filed: 11/30/2001 Examiner: C. Q. Nguyen
Docket No.: TI-31192 Customer No.: 23494
Title: HIGH DENSITY CAPACITOR USING TOPOGRAPHIC SURFACE

CERTIFICATION OF FACSIMILE TRANSMISSION

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Jacqueline J. Garner, Reg. No. 36,144

January 27, 2004
Date

FACSIMILE COVER SHEET

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<input type="checkbox"/> NEW APPLICATION	<input checked="" type="checkbox"/> EOT (3 Pages)
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<input type="checkbox"/> CONTINUATION APP'N (# Pages)	<input checked="" type="checkbox"/> Response (RFR) (3 Pages)
<input type="checkbox"/> DIVISIONAL APP'N	
NAME OF INVENTOR(S): Pan et al.	
TITLE OF INVENTION: HIGH DENSITY CAPACITOR . . .	
Atty. Docket: TI-31192	DEPOSIT ACCT. NO.: 20-0668
FAXED: 1/27/2004 DUE: 10/28/2003 ATTY/SEC'Y: JJG	
RECEIPT DATE & SERIAL NO.: Serial No.: 09/998,606 Filing Date: 11/30/2001 Conf. No.: 4902	

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Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75074



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.: 09/998,606
Applicant: Shanjen Pan et al.
Filed: 11/30/2001
TC/A.U.: 2811
Examiner: Cuong Quang Nguyen
Docket No.: TI-31192
Customer No.: 23494
Title: HIGH DENSITY CAPACITOR USING TOPOGRAPHIC SURFACE

Confirmation No. 4902

REQUEST FOR EXTENSION OF TIME

Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-872-9306 on the date shown below:


Jacqueline J. Garner, Reg. No. 36,144

January 27, 2004
Date

Pursuant to 37 CFR 1.136(a), Applicant(s) respectfully petitions the Commissioner for an extension of the shortened statutory period for response in the above-identified Application.

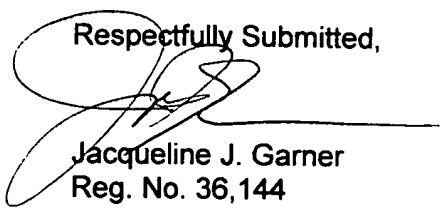
The fee for this extension is indicated below:

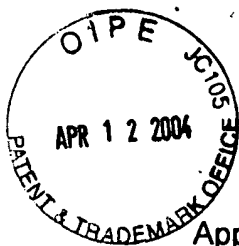
- ☐ One Month (\$110)
☐ Two Months (\$420)
☒ Three Months (\$950)
☐ Four Months (\$1,480)

Please charge the fee to deposit account no. 20-0668. Any further necessary extension of time is hereby requested. Charge any and all fees to deposit account no. 20-0668. An original and two copies of this sheet are enclosed.

Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75265
(214) 532-9348
Fax: (972) 917-4418

Respectfully Submitted,


Jacqueline J. Garner
Reg. No. 36,144



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/998,606 Confirmation No. 4902
Applicant : Shanjen Pan et al.
Filed : 11/30/2001
TC/A.U. : 2811
Examiner : Cuong Quang Nguyen

Docket No. : TI-31192
Customer No. : 23494

Title : HIGH DENSITY CAPACITOR USING TOPOGRAPHIC
SURFACE

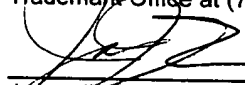
REQUEST FOR RECONSIDERATION UNDER 37 CFR 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Trademark Office at (703) 872 - 9306 on 1/27/2004.


Jacqueline J. Garner
Reg. No. 36,144

The following remarks are offered in response to the Examiner's Office Action dated 07/28/2003. They are respectfully submitted as a full and complete response to that Action.

REMARKS/ARGUMENTS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 18-22 are pending in this case.

The Examiner rejected claims 18-20 under 35 U.S.C. § 103(a) as being unpatentable over Vaartstra (U.S. 6,010,969) in view of Ouellet et al. (U.S. 6,268,620).

Applicant respectfully submits that claim 18 is patentable over Vaartstra in view of Ouellet as there is no disclosure or suggestion in the references of a parallel plate capacitor over a dielectric layer, wherein the parallel plate capacitor extends into and out of a plurality of recesses in the semiconductor layer. Vaartstra teaches a method of forming a film on a semiconductor device using carboxylate complexes. Fig. 1 of Vaartstra shows a memory cell in which a ferroelectric material 11 is formed between two electrodes 12 and 13. The bottom electrode 13 is formed on a silicon-containing layer 14 such as silicon dioxide. While layer 14 extends into recesses in a substrate, as shown in FIG. 1, layer 14 fills the recesses and no part of the capacitor extends into or out of the recesses. The Examiner argues that FIG. 1 of Vaartstra is not drawn to scale and so the capacitor may be extending into and out of recess in a semiconductor. However, in order to properly reject the claims, the prior art must disclose or suggest the claimed invention to one of ordinary skill in the art. While recesses are shown in FIG. 1 of Vaartstra, the recesses are not mentioned in the text of the patent. There is no discussion as to their purpose or depth. As illustrated, the parallel plate capacitor does not extend into and out of recesses in a semiconductor layer and there is no teaching in Vaartstra to suggest modifying a depth of the recess such that a parallel plate capacitor that extends into and out of recesses in a semiconductor layer. Ouellet is added to teach that capacitors are used in memories and analog circuits. Accordingly, Applicant respectfully submits that claim 18 and the claims dependent thereon are patentable over Vaartstra in view of Ouellet.

The Examiner rejected claims 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Vaartstra (U.S. 6,010,969) in view of Ouellet et al. (U.S. 6,268,620) and further in view of Maniar (U.S. 5,185,689).

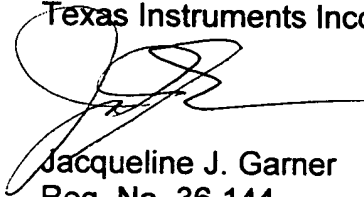
Applicant respectfully submits that claims 21 and 22 are patentable over the references for the same reasons discussed above relative to claim 18 from which these claims depend. Maniar is added to teach PZT as a capacitor dielectric. There is no disclosure or suggestion in the references of a parallel plate capacitor over a dielectric

layer, wherein the parallel plate capacitor extends into and out of a plurality of recesses in the semiconductor layer.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 18-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Texas Instruments Incorporated

A handwritten signature in black ink, appearing to read 'J. Garner', is written over the printed name.

Jacqueline J. Garner

Reg. No. 36,144

Phone: (214) 532-9348

Fax: (972) 917-4418